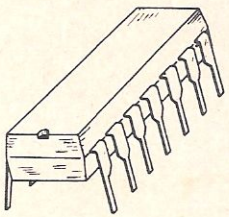
The FC family of DTL silicon monolithic integrated circuits is designed for medium speed digital equipment in computing, telecommunication, instrumentation and industrial control.

NAND GATES

In the standard temperature range the FC family comprises the following NAND gates:

	R_C	non-R_C
Single 8-input NAND gate	FCH111	FCH101
Dual 4-input NAND gate	FCH131	FCH121
Triple 3-3-2-input NAND gate	FCH161	FCH141
Triple 3-input NAND gate	FCH171	FCH151
Quadruple 2-input NAND gate	FCH191	FCH181
Sextuple inverter	FCH211	FCH201



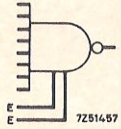
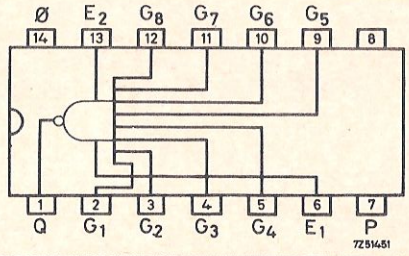
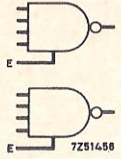
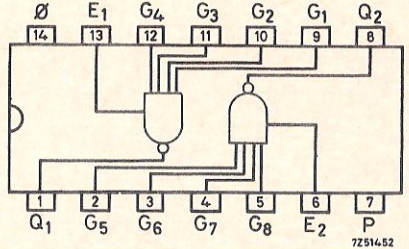
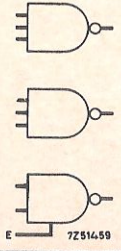
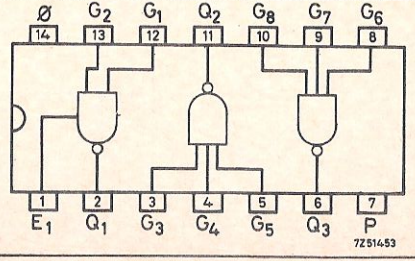
Red binder Integrated circuits

QUICK REFERENCE DATA

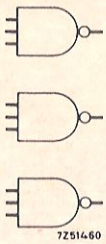
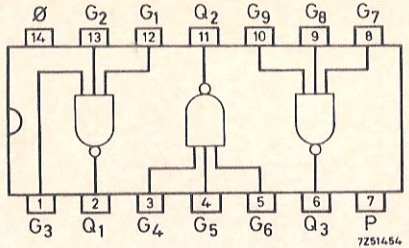
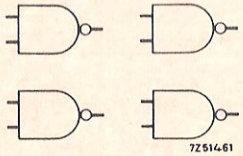
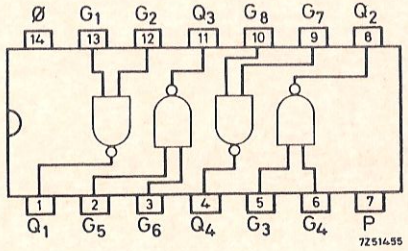
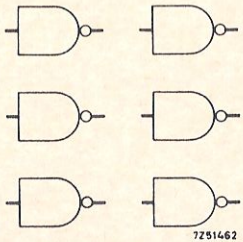
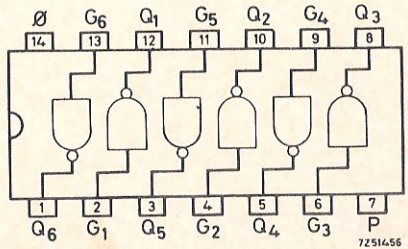
Supply voltage		V_P	6.0 ± 5%	V
Operating ambient temperature range		T_{amb}	0 to 75	°C
Average propagation delay time fan-out = 6; C_W = 60 pF; T_{amb} = 25 °C		t_{pd}	typ. 31	ns
Available fan-out (full temperature range)		N_a	min. 8	
Noise margin at T_{amb} = 25 °C		M_L	min. 0.6 typ. 1.2	V V
Power consumption				
50% duty cycle; T_{amb} = 25 °C	R_C gates	P_{av}	typ. 11	mW
	non-R_C gates	P_{av}	typ. 7	mW
Package			D1 (Dual in-line)	

Features:

- high fan-out (8 at all temperatures between 0 and 75 °C)
- high fan-in capability, expandable by attaching a diode array
- very high d.c. noise margin: 0.4 V min. at worst-case temperature and 1.2 V typ. at 25 °C
- large selection of circuit configurations, including gate types with and without collector resistors, permitting optimum equipment design
- outputs may be interconnected (commoned) for wired-OR function.

Description (positive logic)	Symbol	Type number		Terminal connections (top view)
		R_C	non-R_C	
Single 8-input NAND gate		FCH111	FCH101	
Dual 4-input NAND gate		FCH131	FCH121	
Triple 3-3-2-input NAND gate		FCH161	FCH141	

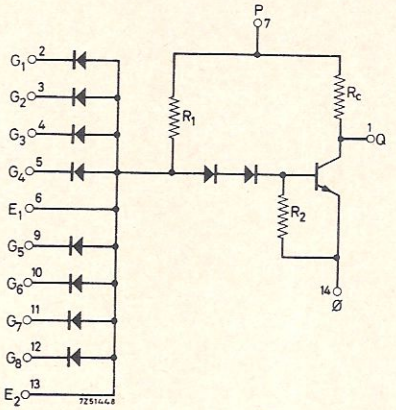
E = Expansion input

Triple 3-input NAND gate		FCH171	FCH151	
Quadruple 2-input NAND gate		FCH191	FCH181	
Sextuple inverter		FCH211	FCH201	

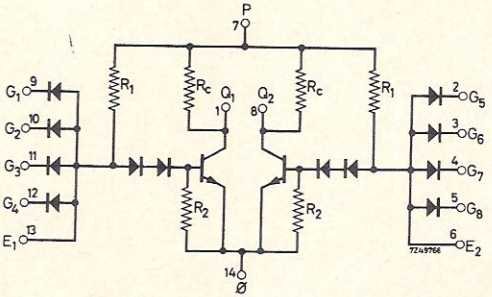
CIRCUIT DIAGRAMS of R_C gates

R_C

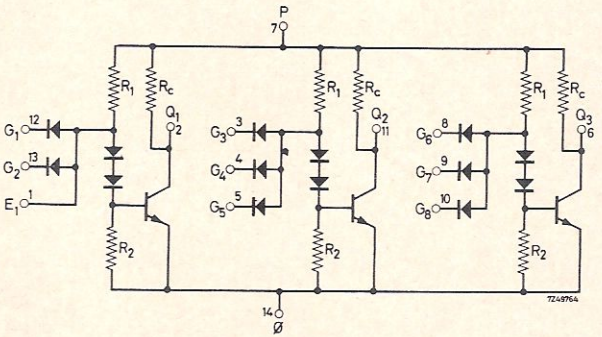
FCH111



FCH131

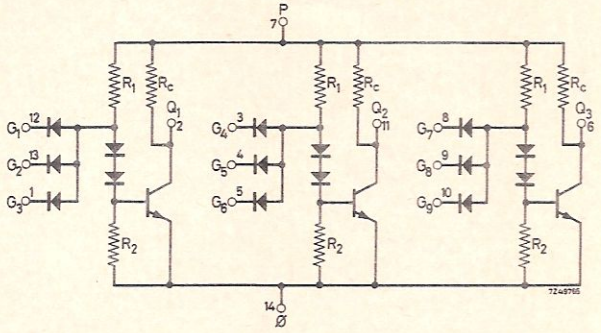


FCH161

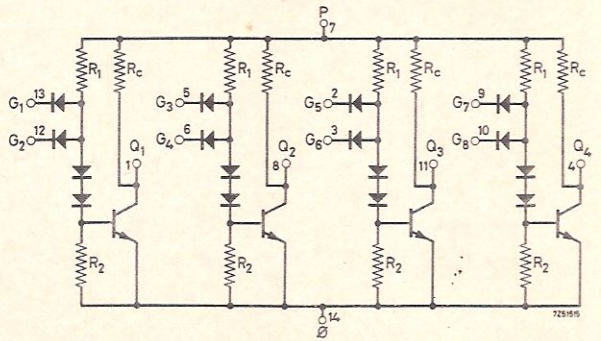


R_C

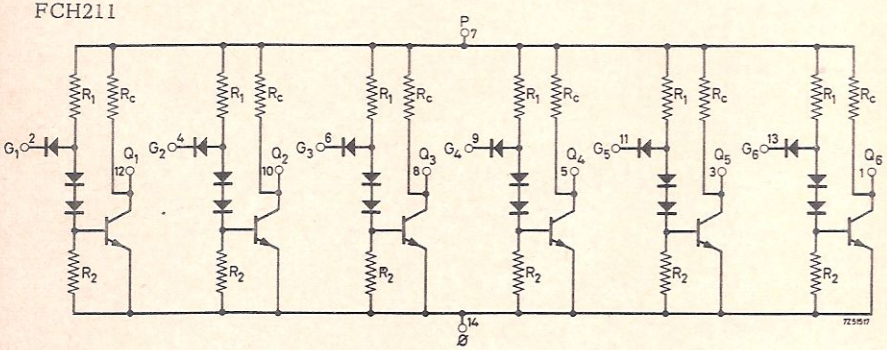
FCH171



FCH191



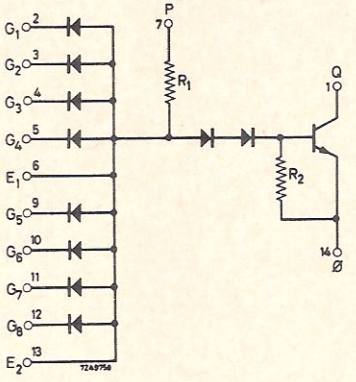
FCH211



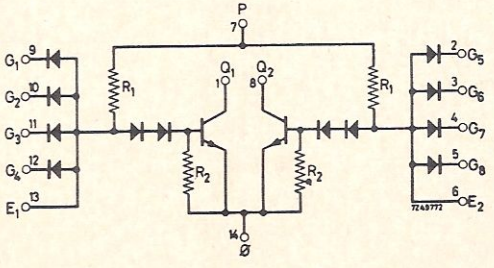
CIRCUIT DIAGRAMS of non-R_C gates

non-R_C

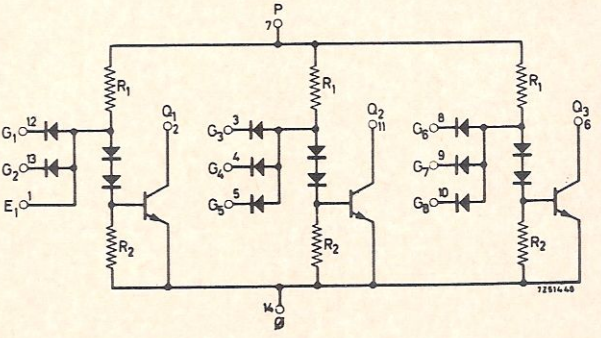
FCH101



FCH121

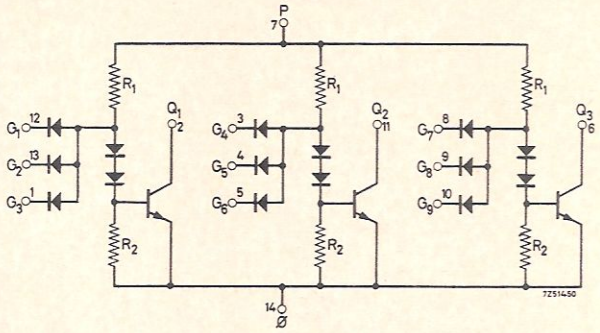


FCH141

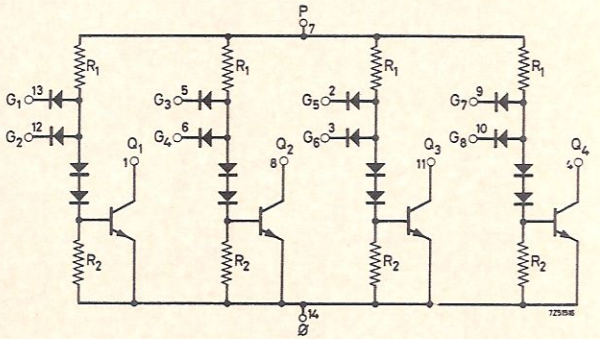


non-R_C

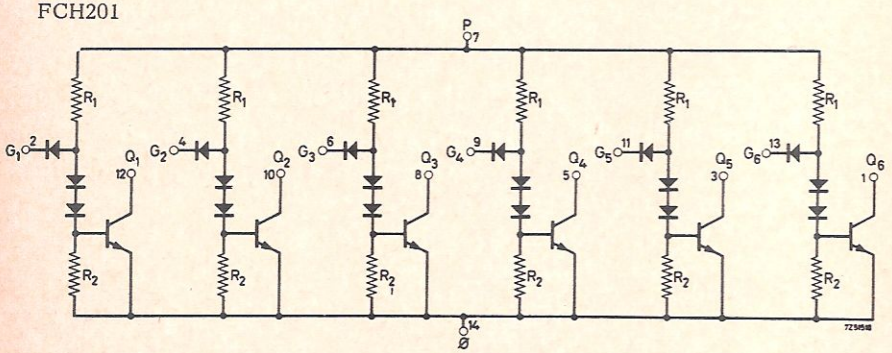
FCH151



FCH181

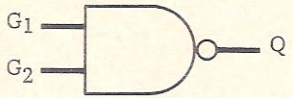


FCH201



LOGIC FUNCTIONS (Positive logic assumed)

Individual gate operation



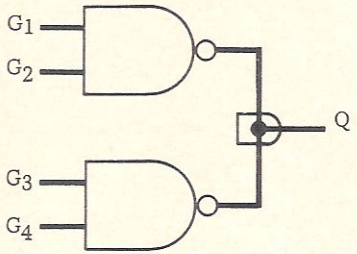
$$Q = \overline{G_1 \cdot G_2}$$

H = HIGH state (the more positive signal voltage)
L = LOW state (the less positive signal voltage)

Function Table

G_1	G_2	Q
L	L	H
L	H	H
H	L	H
H	H	L

Commoned gate operation (wired-OR)



$$Q = \overline{G_1.G_2} \cdot \overline{G_3.G_4} = \overline{G_1.G_2 + G_3.G_4}$$

RATINGS (Limiting values) [1]

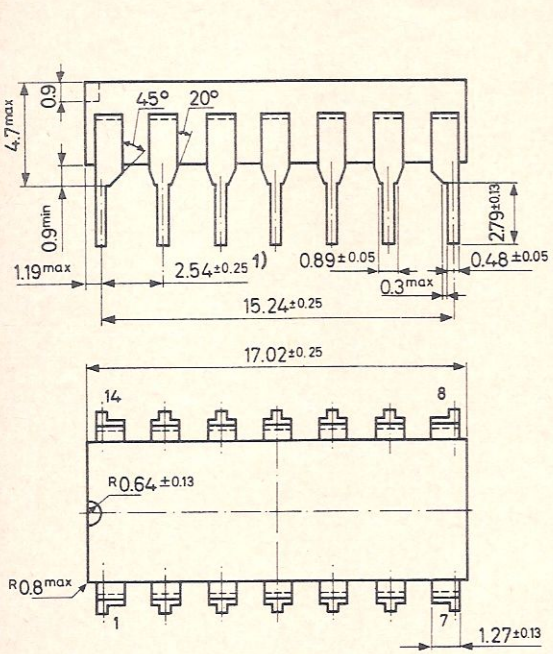
Supply voltage	V_P	max. 10	V
Output voltage	V_Q	0 to 8.0	V
G input voltage	V_G	max. 8.0	V
Neg. G input current	$-I_G$	max. 20	mA [2]
Neg. E input voltage at $V_G \leq 6.3$ V	$-V_E$	max. 1.0	V
E input current	I_E	max. 5.0	mA
Storage temperature	T_{stg}	−35 to +125	°C
Operating ambient temperature	T_{amb}	0 to +75	°C

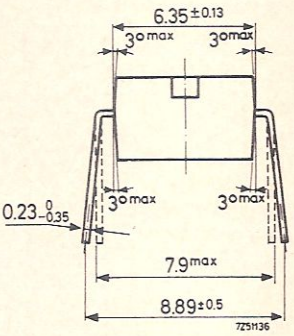
[1] Limiting values according to the Absolute Maximum System as defined in IEC publication 134.

[2] At this limit $-V_G$ typ. 0.6 V.

PACKAGE OUTLINE

Dimensions in mm





Top view

1) Tolerance non-cumulative

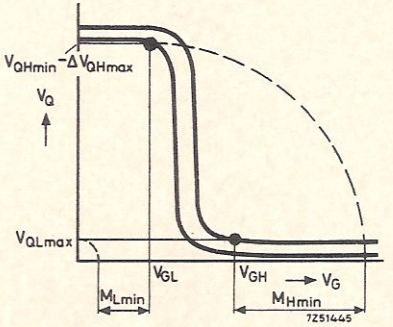
INTRODUCTION TO THE CHARACTERISTICS

1. General assumptions

- All voltages are assumed to be measured with respect to the reference terminal, designated by $\emptyset$.
- A current is taken as positive when its conventional direction of flow is into the device.
- Where no electrical conditions are specified for a given terminal, it is left unconnected.
- Conditions such as "Input V_{QLmax}" are to be understood as follows: for each temperature, the maximum value of the voltage V_{QL} is applied to the input.

2. Input threshold voltage levels V_{GL} and V_{GH}. Output current I_{QL}

At input voltages equal to the threshold voltage levels V_{GL} and V_{GH}, the circuit is near the limit of switching. V_{GL} and V_{GH}, therefore, describe a specific property of the circuit.
They are defined together with V_{QLmax} and (V_{QHmin} - ΔV_{QHmax}) by two points of the worst-case voltage transfer curves.



I_{QL} is the value of LOW state output current at and below which V_Q will not exceed V_{QLmax}.
V_{GL}, V_{GH} and I_{QL} are defined as being independent of any condition except temperature, thus forming the basis of the other circuit variables.

Page 11 is missing from data sheet.

R_C

CHARACTERISTICS of R_C gates

	Electrical conditions				T_{amb} (°C)			
	input G	output Q	supply P		0	+25	+75	
STATIC DATA								
Input threshold voltage levels								
- input LOW	–	–	–	V_{GL}	1.0	1.0	0.8	V
- input HIGH	–	–	–	V_{GH}	2.3	2.2	2.1	V
Output voltage levels								
- output LOW	V_{GH}	I_{QL}	5.7 V	V_{QL} max.	0.4	0.4	0.4	V
- output HIGH, unloaded	V_{GL}	$I_Q = 0$	5.7 V	V_{QH} min.	5.3	5.3	5.3	V
- output HIGH, voltage drop with loading	V_{GL}	I_Q = a μA	5.7 V	ΔV_{QH} max.	a x 6.0	a x 6.0	a x 7.0	mV
Output currents								
- output LOW input HIGH	–	–	–	I_{QL}	14.0	13.2	12.4	mA
- output LOW input LOW (wired-OR) [1]	V_{QLmax}	V_{QLmax}	6.3 V	$-I_{QLL}$ max.	2.2	2.1	2.0	mA
Input currents [2]								
- input LOW	V_{QLmax}	–	5.7 V	$-I_{GL}$ max.	1.75	1.65	1.55	mA
			6.3 V	$-I_{GL}$ max.	2.0	1.9	1.8	mA
- input HIGH	V_{QHmin}; other inputs $V_G = 0$		5.7 V	I_{GH} max.	1.0	1.0	25	μA

1) Output forced LOW externally, as in the case of collector-OR operation.

2) In case of expansion input: identical values, provided a diode is inserted whose characteristics are similar to those of the FCY101.

CHARACTERISTICS of R_c gates (continued)

R_c

	supply P			T_{amb} (°C) 0	+25	+75	
DYNAMIC DATA							
Time reference level	–	V_{pd}		1.5	1.5	1.5	V
Rise propagation delay time N = 1; C_w = 40 pF	6.0 V	t_{pdr}	typ.	47	50	56	ns
			max.		85		ns
N = 6; C_w = 60 pF	6.0 V	t_{pdr}	typ.	28	30	34	ns
			max.		70		ns
Fall propagation delay time N = 1; C_w = 40 pF	6.0 V	t_{pdf}	typ.	26	26	28	ns
			max.		65		ns
N = 6; C_w = 60 pF	6.0 V	t_{pdf}	typ.	33	32	32	ns
			max.		85		ns
Input capacitance (equiv.)	6.0 V	C_G	typ.		7		pF
Output capacitance (equiv.)	6.0 V	C_Q	typ.		25		pF
Collector resistor	–	R_c	typ.	4.3	4.4	5.0	kΩ
SUPPLY							
Supply current							
- Output LOW, input HIGH	6.0 V	I_{PL}	typ.	2.6	2.4	2.3	mA
	6.3 V	I_{PL}	max.	4.2	3.8	3.6	mA
- Output HIGH, input LOW	6.0 V	I_{PH}	typ.	1.3	1.25	1.2	mA
	6.3 V	I_{PH}	max.	2.0	1.9	1.8	mA
DERIVED DATA							
Available d.c. fan-out to similar circuits	5.7 V	N_a	min.	8	8	8	
D.C. Noise margins							
- LOW	5.7 V	M_L	min.	0.6	0.6	0.4	V
- HIGH	5.7 V	M_H	min.	2.9	3.0	1.8	V
Power supply consumption (50% duty cycle)	6.0 V	P_{av}	typ.	12	11	10.5	mW
	6.3 V	P_{av}	max.	20	18	17	mW
Average propagation delay time $\frac{t_{pdr} + t_{pdf}}{2}$							
N = 1; C_w = 40 pF	6.0 V	t_{pd}	typ.	37	38	42	ns
N = 6; C_w = 60 pF	6.0 V	t_{pd}	typ.	31	31	33	ns

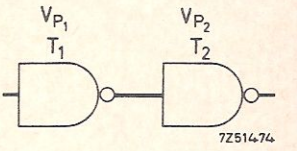
ADDITIONAL SYSTEM DESIGN DATA of R_C gates

R_C

In addition to the basic information contained in the Characteristics, the following data provides extended aid to optimum system design.
Except for section 1.1, all values given are guaranteed limits.

Legend: A = number of commoned R_C gates
B = number of commoned non-R_C gates
I_{leak} = total LOW state diode leakage current through inputs other than those driven by the gate concerned.
} see Fig.8

V_{P1} = supply voltage of driving gate
V_{P2} = supply voltage of driven gate
T_1 = ambient temperature of driving gate
T_2 = ambient temperature of driven gate
T_{av} = average ambient temp.: $\frac{T_1 + T_2}{2}$



1. CONDITIONS: A = 0, B = 0, I_{leak} = 0

1.1 Propagation delay versus wiring capacitance (Fig.1 and 2)

Conditions: V_P = 6.0 V T_{amb} = 25 °C

V_{pd} and test setup as quoted in Characteristics

1.2 Fan-out versus temperature

1.2.1 Supply voltage difference = 0 and temperature difference = 0 (Fig. 3, T_{amb})

Conditions: $V_{P1} = V_{P2}$ = 5.7 to 6.3 V $T_1 = T_2$

1.2.2 Supply voltage difference ≤ 0.3 V and temperature difference = 0

Conditions: V_{P1} = 5.7 to 6.3 V $|V_{P1} - V_{P2}| \leq 0.3$ V (Fig. 3; T_{amb})
V_{P2} = 5.7 to 6.3 V $T_1 = T_2$

1.2.3 Supply voltage difference ≤ 0.3 V and temperature difference = 30 °C [1])

Conditions: V_{P1} = 5.7 to 6.3 V $|V_{P1} - V_{P2}| \leq 0.3$ V (Fig. 3, T_{av})
V_{P2} = 5.7 to 6.3 V $|T_1 - T_2| = 30$ °C

1.2.4 Supply voltage difference ≤ 0.3 V and temperature difference ≤ 75 °C

Conditions: V_{P1} = 5.7 to 6.3 V $|V_{P1} - V_{P2}| \leq 0.3$ V
V_{P2} = 5.7 to 6.3 V $|T_1 - T_2| \leq 75$ °C

Result: available fan-out $N_{amin} = 6$

1) Since a temperature difference of 30 °C is specified, T_{av} of 15 to 60 °C will include the entire range of 0 to 75 °C, because $T_{av} = \frac{T_1 + T_2}{2}$

R_C

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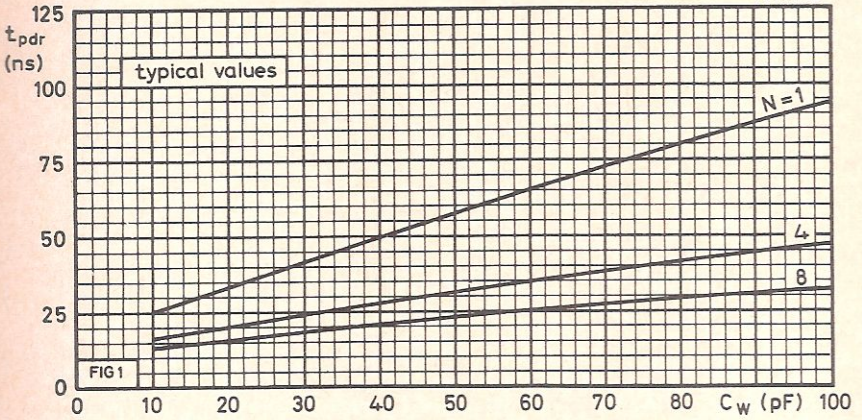

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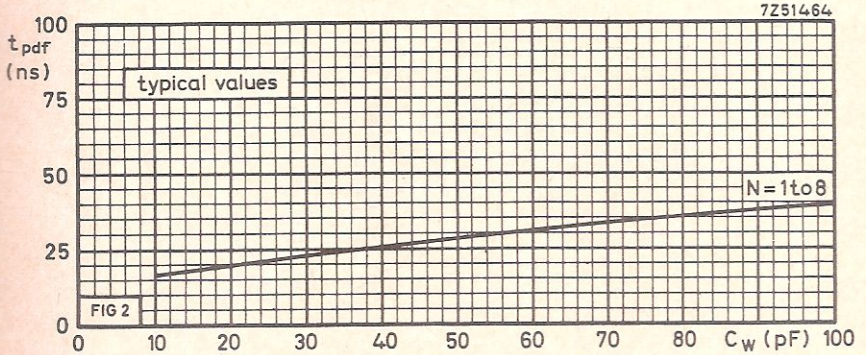

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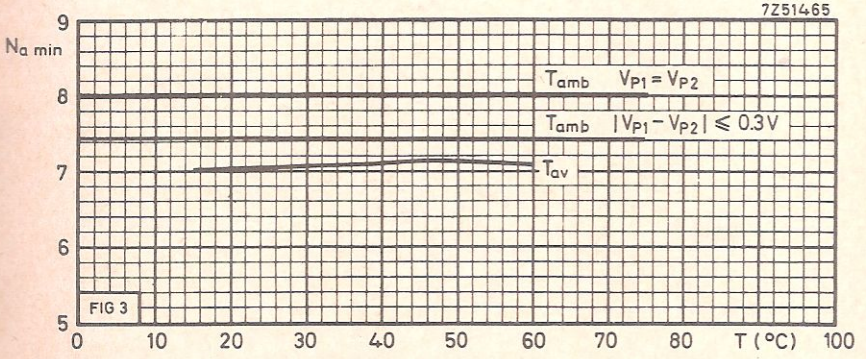


R_c

1.3 Noise margins versus temperature

1.3.1 Supply voltage difference $\leq$ 0.6 V (Fig.4)

Conditions: V_{P1} = 5.7 to 6.3 V N = 1 to 8
V_{P2} = 5.7 to 6.3 V

Note: V_{QHmin} * = minimum value of V_{QH} for worst-case HIGH state load current, being 8 x 25 μA = 200 μA (i.e., for calculating ΔV_{QH} : a = 200)

As illustration the values of M_{Lmin} and M_{Hmin} have been derived for T_1 = 30 °C, T_2 = 70 °C, in Fig.4.
It may also be seen from Fig.4 that the worst cases are:

M_{Lmin} = 0.4 V (T_1 = 0 to 75 °C; T_2 = 75 °C)

M_{Hmin} = 1.6 V (T_1 = 75 °C; T_2 = 0 °C)

1.3.2 Supply voltage difference $\leq$ 0.6 V and temperature difference = 0
(Fig.5, T_{amb})

Conditions: V_{P1} = 5.6 to 6.3 V $T_1 = T_2$
V_{P2} = 5.7 to 6.3 V N = 1 to 8

1.3.3 Supply voltage difference $\leq$ 0.6 V and temperature difference = 30 °C
(Fig.5; T_{av})

Conditions: V_{P1} = 5.7 to 6.3 V $|T_1 - T_2|$ = 30 °C
V_{P2} = 5.7 to 6.3 V N = 1 to 7

R_C

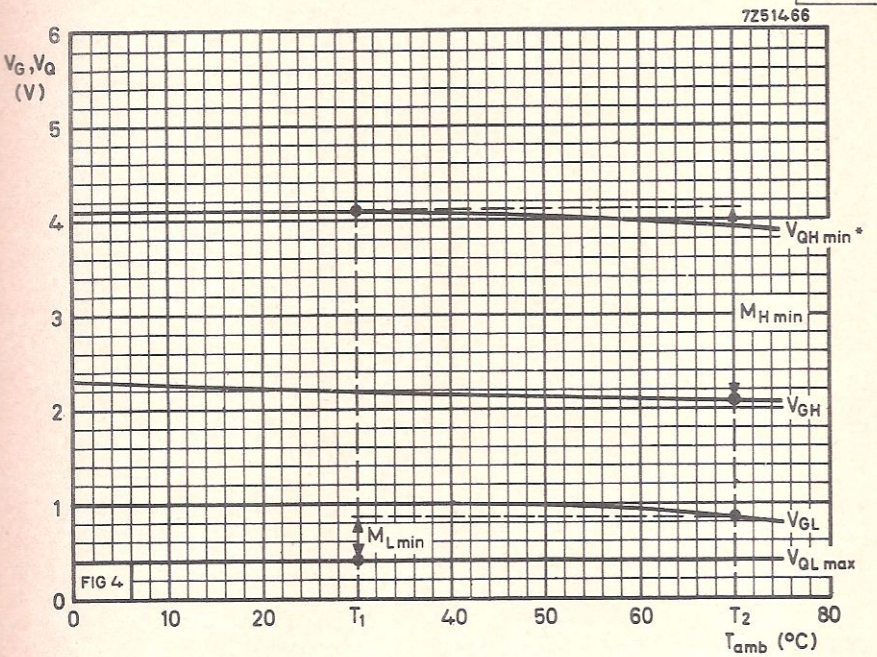

7Z51466
V_G, V_Q (V)
$V_{QH\ min}$ *
$M_{H\ min}$
V_{GH}
V_{GL}
$M_{L\ min}$
$V_{QL\ max}$
T_1
T_2
T_{amb} (°C)

FIG 4

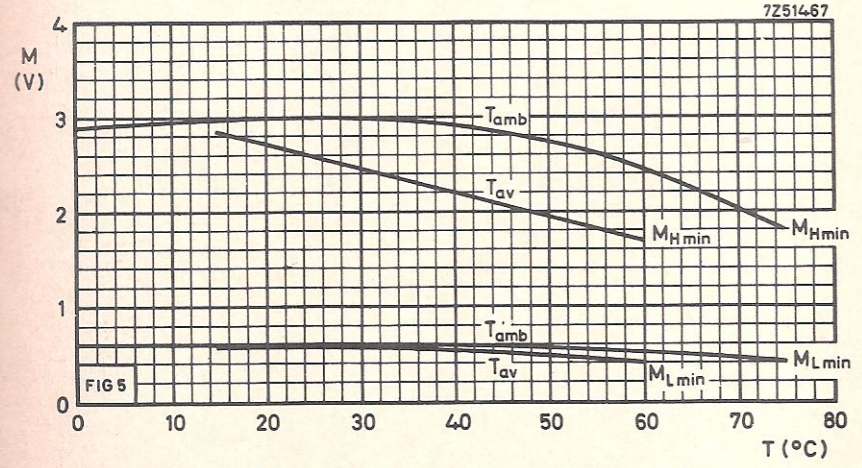

7Z51467
M (V)
T_{amb}
T_{av}
$M_{H\ min}$
$M_{H\ min}$
T_{amb}
T_{av}
$M_{L\ min}$
$M_{L\ min}$
T (°C)

FIG 5

2. CONDITIONS: A ≠ 0 or B ≠ 0 or $I_{leak} \neq 0$ V_P = 5.7 to 6.3 V

R_C

For any two gates: Supply voltage difference ≤ 0.3 V
Temperature difference = 0

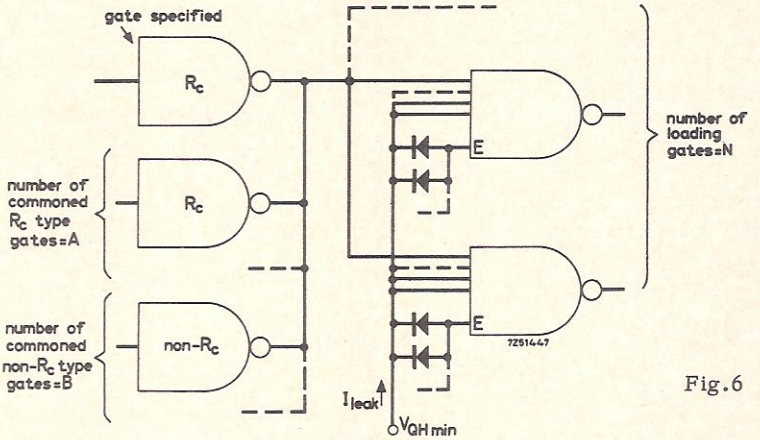
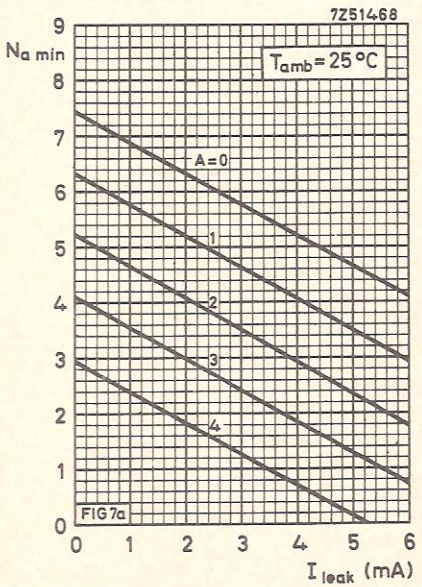
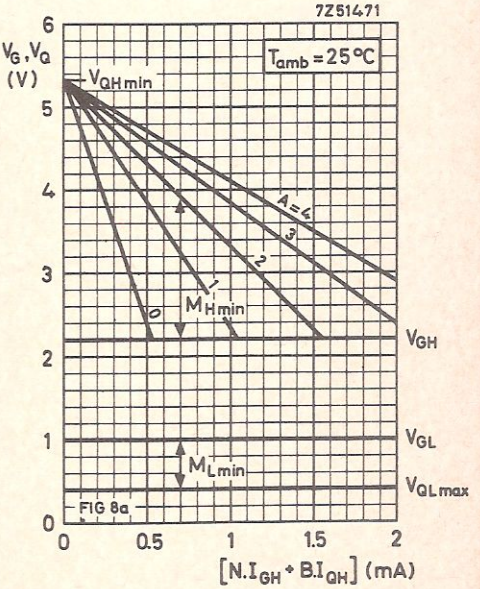


Fig.6

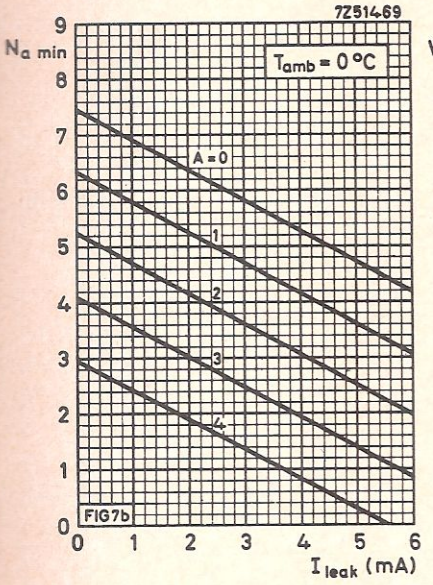
2.1 Fan out N_a depends on A and I_{leak}

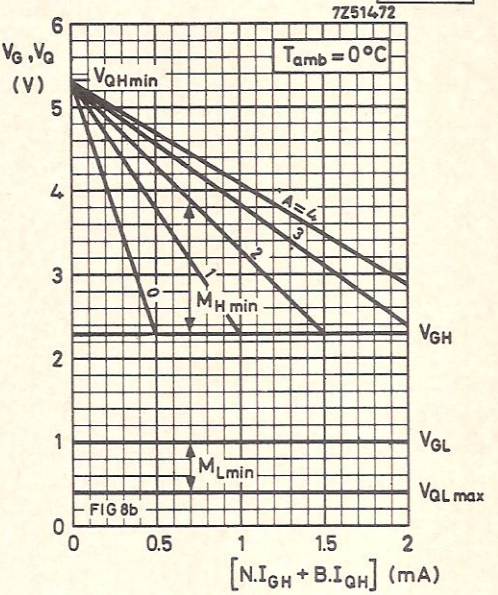
2.2 Noise margin M_H depends on A, B, N, I_{GH} (HIGH state input current of loading gates) and I_{QH} (HIGH state output current of commoned non-R_C gates). M_L is not affected.

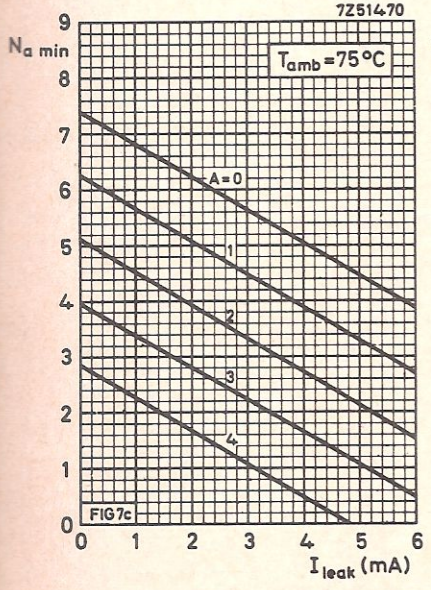


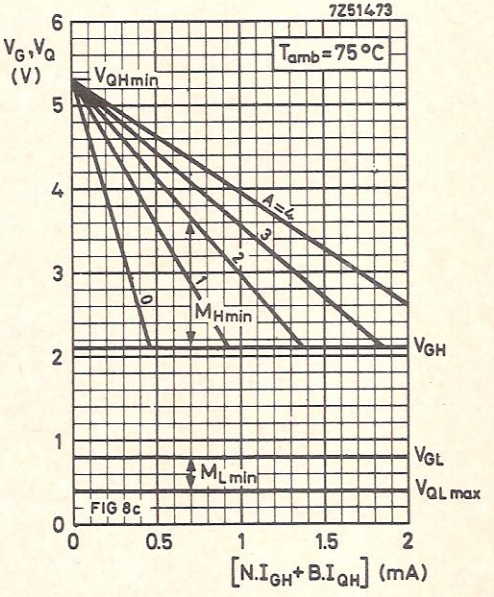


R_C


7Z51469
N_a min
T_{amb} = 0 °C
A = 0
1
2
3
4
FIG 7b
I_{leak} (mA)


7Z51472
V_G, V_Q (V)
T_{amb} = 0 °C
$V_{QH\,min}$
A = 4
3
2
1
0
$M_{H\,min}$
V_{GH}
V_{GL}
$M_{L\,min}$
$V_{QL\,max}$
FIG 8b
$[N.I_{GH} + B.I_{QH}]$ (mA)


7Z51470
N_a min
T_{amb} = 75 °C
A = 0
1
2
3
4
FIG 7c
I_{leak} (mA)


7Z51473
V_G, V_Q (V)
T_{amb} = 75 °C
$V_{QH\,min}$
A = 4
3
2
1
0
$M_{H\,min}$
V_{GH}
V_{GL}
$M_{L\,min}$
$V_{QL\,max}$
FIG 8c
$[N.I_{GH} + B.I_{QH}]$ (mA)

CHARACTERISTICS of non-R_c gates

non-R_c

	Electrical conditions				T_{amb} (°C)			
	input G	output Q	supply P		0	+25	+75	
STATIC DATA								
Input threshold voltage levels								
- input LOW	-	-	-	V_{GL}	1.0	1.0	0.8	V
- input HIGH	-	-	-	V_{GH}	2.3	2.2	2.1	V
Output voltage level								
- output LOW	V_{GH}	I_{QL}	5.7 V	V_{QL} max.	0.4	0.4	0.4	V
Output currents								
- output LOW	-	-	-	I_{QL}	16.0	15.1	14.2	mA
- output HIGH	V_{GL}	5.3 V	6.3 V	I_{QH} max.	70	70	70	µA
Input currents *)								
- input LOW	V_{QL}max	-	5.7 V 6.3 V	$-I_{GL}$ max. $-I_{GL}$ max.	1.75 2.0	1.65 1.9	1.55 1.8	mA mA
- input HIGH	5.3 V; other inputs V_G = 0	-	5.7 V	I_{GH} max.	1.0	1.0	25	µA

*) In case of expansion input: identical values, provided a diode is inserted whose characteristics are similar to those of the FCY101.

CHARACTERISTICS of non-R_c gates (continued)

non-R_c

	supply P			T_{amb} (°C) 0	+25	+75	
DYNAMIC DATA **)							
Time reference level	-	V_{pd}	•	1.5	1.5	1.5	V
Rise propagation delay time N = 1; C_w = 40 pF	6.0 V	t_{pdr}	typ.	47	50	56	ns
			max.		85		ns
N = 6; C_w = 60 pF	6.0 V	t_{pdr}	typ.	28	30	34	ns
			max.		70		ns
Fall propagation delay time N = 1; C_w = 40 pF	6.0 V	t_{pdf}	typ.	26	26	28	ns
			max.		65		ns
N = 6; C_w = 60 pF	6.0 V	t_{pdf}	typ.	33	32	32	ns
			max.		85		ns
Input capacitance (equiv.)	6.0 V	C_G	typ.		7		pF
Output capacitance (equiv.)	6.0 V	C_Q	typ.		25		pF
SUPPLY							
Supply current							
- Output LOW, input HIGH	6.0 V	I_{PL}	typ.	1.3	1.15	1.2	mA
	6.3 V	I_{PL}	max.	2.0	1.7	1.6	mA
- Output HIGH, input LOW	6.0 V	I_{PH}	typ.	1.3	1.25	1.2	mA
	6.3 V	I_{PH}	max.	2.0	1.9	1.8	mA
DERIVED DATA							
Available d.c. fan-out to similar circuits **)	5.7 V	N_a	min.	8	8	8	
D.C. Noise margins **)							
- LOW	5.7 V	M_L	min.	0.6	0.6	0.4	V
- HIGH	5.7 V	M_H	min.	2.9	3.0	1.8	V
Power supply consumption (50% duty cycle)	6.0 V	P_{av}	typ.	8	7	7	mW
	6.3 V	P_{av}	max.	13	11	11	mW
Average propagation delay time $\frac{t_{pdr} + t_{pdf}}{2}$ **)							
N = 1; C_w = 40 pF	6.0 V	t_{pd}	typ.	37	38	42	ns
N = 6; C_w = 60 pF	6.0 V	t_{pd}	typ.	31	31	33	ns

**) With external collector resistor similar to that included in R_c gates.

ADDITIONAL SYSTEM DESIGN DATA of non-R_C gates

non-R_C

Non-R_C gates are intended to be commoned to R_C gates, for optimum use of the wired-OR feature. Therefore, the Additional System Design Data as specified for R_C gates also applies to non-R_C gates, provided the output of the non-R_C gate is connected to the output of an R_C gate whose input state is LOW.